PIC12(L)F1840 Family
Silicon Errata and Data Sheet Clarification

The PIC12(L)F1840 family devices that you have received conform functionally to the current Device Data Sheet (DS40001441**F**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC12(L)F1840 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A5**).

Data Sheet clarifications and corrections start on page 8, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC12(L)F1840 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)	
		A4	A5
PIC12F1840	01 1011 100	0 0100	0 0101
PIC12LF1840	01 1011 110	0 0100	0 0101

Note 1: The Device ID is located in the configuration memory at address 8006h.

2: Refer to the *"PIC16F/LF1847/PIC12F/LF1840 Memory Programming Specification"* (DS41439) for detailed information on Device and Revision IDs for your specific device.

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TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)	
				A4	A5
Oscillator	Clock Switching	1.1	Clock switching fails	X	
Oscillator	Oscillator Start-up Timer	1.2	OSTS bit remains clear when 4xPLL enabled.	X	X
Oscillator	Oscillator Start-up Timer	1.3	OSTS bit remains set.	X	
Master Synchronous Serial Port (MSSP)	SPI Master mode	2.1	Buffer Full (BF) bit or MSSP Interrupt Flag (SSPIF) bit becomes set half SCK cycle too early.	X	X
Master Synchronous Serial Port (MSSP)	SPI Slave mode	2.2	SPI master releasing Slave Select during Slave Sleep mode corrupts data.	X	X
Master Synchronous Serial Port (MSSP)	SPI Slave mode	2.3	SPI master enabling Slave Select too early could lose received data in Slave mode.	X	X
Master Synchronous Serial Port (MSSP)	SPI Slave mode	2.4	WCOL is erroneously set in SPI Slave mode during Sleep.	X	X
EUSART	Auto-Baud Detect	3.1	Auto-Baud Detect may store incorrect count value in the SPBRG registers.	X	
LDO	Low-Power Sleep mode	4.1	Unexpected Resets may occur at ambient temperatures below 0°C.	X	
Fixed Voltage Reference (FVR)	Gain Amplifier Output	5.1	Use of FVR module can cause device Reset.	X	X
ECCP	Compare mode	6.1	Compare Toggle mode yields unexpected results.	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

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Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A5**).

1. Module: Oscillator

1.1 Clock Switching

When switching clock sources between INTOSC clock source and an external clock source operating at a different power mode, one corrupted instruction may be executed after the switch occurs.

This issue does not affect Two-Speed Start-up or the Fail-Safe Clock Monitor operation.

Work around

When clock switching from an external oscillator clock source, first switch to 16 MHz HFINTOSC. Once running at 16 MHz HFINTOSC, configure IRCF to run at desired frequency.

When clock switching from an INTOSC to an external oscillator clock source, first switch from desired INTOSC frequency to HFINTOSC High-Power mode (8 MHz or 16 MHz). Once running from HFINTOSC, switch to the external oscillator clock source.

Affected Silicon Revisions

A4	A5						
X							

1.2 Oscillator Start-up Timer

When the 4xPLL is enabled, the Oscillator Start-up Timer Status (OSTS) bit always remains clear.

Work around

None.

Affected Silicon Revisions

A4	A5						
X	X						

1.3 Oscillator Start-up Timer (OST) Bit

During the Two-Speed Start-up sequence, the OST is enabled to count 1024 clock cycles. After the count is reached, the OSTS bit is set, the system clock is held low until the next falling edge of the external crystal (LP, XT or HS mode), before switching to the external clock source.

When an external oscillator is configured as the primary clock and Fail-Safe Clock mode is enabled (FCMEN = 1), any of the following conditions will result in the Oscillator Start-up Timer (OST) failing to restart:

- $\overline{\text{MCLR}}$ Reset
- Wake from Sleep
- Clock change from INTOSC to Primary Clock

This anomaly will manifest itself as a clock failure condition for external oscillators, which take longer than the clock failure time-out period to start.

Work around

None.

Affected Silicon Revisions

A4	A5						
X							

2. Module: Master Synchronous Serial Port (MSSP)

2.1 SPI Master mode

When the MSSP is used in SPI Master mode and the CKE bit is clear (CKE = 0), the Buffer Full (BF) bit and the MSSP Interrupt Flag (SSPIF) bit becomes set half an SCK cycle early. If the user software immediately reacts to either of the bits being set, a write collision may occur as indicated by the WCOL bit being set.

Work around

To avoid a write collision one of the following methods should be used:

Method 1: Add a software delay of one SCK period after detecting the completed transfer (the BF bit or SSPIF bit becomes set) and prior to writing to the SSP1BUF register. Verify the WCOL bit is clear after writing to SSP1BUF. If the WCOL bit is set, clear the bit in software and rewrite the SSP1BUF register.

Method 2: As part of the MSSP initialization procedure, set the CKE bit (CKE = 1).

Affected Silicon Revisions

A4	A5						
X	X						

2.2 SPI Slave Mode

When the MSSP module is configured in SPI Slave mode with $\overline{SS}$ pin control enabled (SSPM = 0100) and the device is in Sleep mode during SPI activity, if the SPI master releases the $\overline{SS}$ line ($\overline{SS}$ goes high) before the device wakes from Sleep and updates SSP1BUF, the received data will be lost.

Work around

Method 1: The SPI master must wait a minimum of parameter SP83 (1.5 TCY + 40 ns) after the last SCK edge and the additional wake-up time from Sleep (device dependent) before releasing the $\overline{SS}$ line.

Method 2: If both the master and slave devices have an available pin, once the slave has completed the transaction and BF or SSPIF is set, the slave could toggle an output to inform the master that the transaction is complete and that it is safe to release the $\overline{SS}$ line.

Affected Silicon Revisions

A4	A5						
X	X						

2.3 SPI Slave Mode

When the MSSP module is configured in SPI Slave mode with $\overline{SS}$ pin control enabled (SSPM = 0100) and the device is in Sleep mode during SPI activity, if the SPI master enables $\overline{SS}$ ($\overline{SS}$ goes low) within 1 TCY before Sleep is executed, the data written into the SSP1BUF by the slave for transmission will remain in the SSP1BUF, and the byte received by the slave will be completely discarded. The MSb of the data byte that is currently loaded into SSP1BUF will be transmitted on each of the eight SCK clocks, resulting in either a 0x00 or 0xFF address to be incorrectly transmitted. This issue typically occurs when the device wakes up from Sleep to process data and immediately goes back to Sleep during the next transmission.

Work around

The SPI slave must wait a minimum of 2.25 * TCY from the time the $\overline{SS}$ line becomes active ($\overline{SS}$ goes low) before executing the Sleep command.

Affected Silicon Revisions

A4	A5						
X	X						

2.4 SPI Slave Mode

When the MSSP module is configured with either of the Slave modes listed below and Sleep is executed during transmission, the WCOL bit is erroneously set. Although the WCOL is set, it does not cause a break in transmission or reception.

Mode 1: SPI Slave mode with $\overline{SS}$ disabled (SSPM = 0101) and CKE = 0.

Mode 2: SPI Slave mode with $\overline{SS}$ enabled (SSPM = 0100) and $\overline{SS}$ not set and then cleared before each consecutive transmission. This typically occurs during multiple byte transmissions in which the master does not release the $\overline{SS}$ line until all transmission has completed.

Work around

Method 1: The WCOL bit can be ignored since the issue does not interfere with MSSP hardware.

Method 2: Clear the SSPEN bit after each transaction, then set SSPEN before next transaction.

Affected Silicon Revisions

A4	A5						
X	X						

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3. Module: EUSART

3.1 Auto-Baud Detect

When using automatic baud detection (ABDEN), on occasion an incorrect count value can be stored at the end of auto-baud detection in the SPBRGH:SPBRGL (SPBRG) registers. The SPBRG value may be off by several counts. This condition happens sporadically when the device clock frequency drifts to a frequency where the SPBRG value oscillates between two different values. The issue is present regardless of the baud rate Configuration bit settings.

Work around

When using auto-baud, it is a good practice to always verify the obtained value of SPBRG, to ensure it remains within the application specifications. Two recommended methods are shown below.

For additional auto-baud information, refer to the technical brief TB3069, *"Use of Auto-Baud for Reception of LIN Serial Communications Devices: Mid-Range and Enhanced Mid-Range"* (DS93069).

EXAMPLE 1: METHOD 1 – EUSART AUTO-BAUD DETECT WORK AROUND

```
#define SPBRG_16BIT *((*int)&SPBRG;    // define location for 16-bit SPBRG value
const int DEFAULT_BAUD = 0x0067;       // Default Auto-Baud value
const int TOL = 0x05;                  // Baud Rate % tolerance
const int MIN_BAUD = DEFAULT_BAUD - TOL;// Minimum Auto-Baud Limit
const int MAX_BAUD = DEFAULT_BAUD + TOL;// Maximum Auto-Baud Limit
   •
   •
   •
ABDEN = 1;                             // Start Auto-Baud
while (ABDEN);                         // Wait until Auto-Baud completes

if((SPBRG_16BIT > MAX_BAUD)||(SPBRG_16BIT < MIN_BAUD))
{                                      // Compare if value is within limits
    SPBRG_16BIT = DEFAULT_BAUD);       // if out of spec, use DEFAULT_BAUD
}
       •                               // if in spec, continue using the
       •                               // Auto-Baud value in SPBRG
       •
```

Note: In firmware, define default, minimum and maximum auto-baud (SPBRG) values according to the application requirements. For example, if the application runs at 9600 baud at 16 MHz, then the default SPBRG value would be (assuming 16-bit/Asynchronous mode) 0x67. The minimum and maximum allowed values can be calculated based on the application. In this example, a ±5% tolerance is required, so tolerance is 0x67 x 5% = 0x05.

EXAMPLE 2: METHOD 2 – EUSART AUTO-BAUD DETECT WORK AROUND

```
#define SPBRG_16BIT *((*int)&SPBRG;        // define location for 16-bit SPBRG value

const int DEFAULT_BAUD = 0x0067;           // Default Auto-Baud value
const int TOL = 0x05;                      // Baud Rate % tolerance
const int MIN_BAUD = DEFAULT_BAUD - TOL;   // Minimum Auto-Baud Limit
const int MAX_BAUD = DEFAULT_BAUD + TOL;   // Maximum Auto-Baud Limit

int Average_Baud;                          // Define Average_Baud variable
int Integrator;                            // Define Integrator variable
   •
   •
   •
Average_Baud = DEFAULT_BAUD;               // Set initial average Baud rate
Integrator = DEFAULT_BAUD*15;              // The running 16 count average
   •
   •
   •
ABDEN = 1;                                 // Start Auto-Baud
while (ABDEN);                             // Wait until Auto-Baud completes

Integrator+ = SPBRG_16BIT;
Average_Baud = Integrator/16;
if((SPBRG_16BIT > MAX_BAUD)||(SPBRG_16BIT < MIN_BAUD))
{                                          // Check if value is within limits
    SPBRG_16BIT = Average_Baud;            // If out of spec, use previous average
}
else                                       // If in spec, calculate the running
{                                          // average but continue using the
    Integrator+ = SPBRG_16BIT;             // Auto-Baud value in SPBRG
    Average_Baud = Integrator/16;
    Integrator- = Average_Baud;
}
   •
   •
   •
```

Note: Similar to Method 1, define default, minimum and maximum auto-baud (SPBRG) values. In firmware, compute a running average of SPBRG. If the new SPBRG value falls outside the minimum or maximum limits, then use the current running average value (Average_Baud), otherwise use the auto-baud SPBRG value and calculate a new running average. For example, if the application runs at 9600 baud at 16 MHz, then the default SPBRG value would be (assuming 16-bit/Asynchronous mode) 0x67. The minimum and maximum allowed values can be calculated based on the application. In this example, a ±5% tolerance is required, so tolerance is 0x67 x 5% = 0x05.

Affected Silicon Revisions

A4	A5						
X							

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4. Module: LDO

4.1. Low-Power Sleep Mode

On very rare occasions, and under the below conditions, the LDO voltage will drop below the minimum V_{DD}, causing unexpected device Resets.

1. Ambient temperatures below 0°C
2. While in Sleep mode
3. VREGCON configured for Low-Power Sleep mode (V_{REGPM} = 1)

Work around

For applications that operate at ambient temperatures below 0°C, use the LDO voltage regulator in Normal Power mode (V_{REGPM} = 0).

Affected Silicon Revisions

A4	A5						
X							

5. Module: Fixed Voltage Reference (FVR)

5.1 Gain Amplifier Output

When using the FVR module, if the gain amplifier outputs are set via the CDAFVR or ADFVR bits in FVRCON while the module is disabled (FVREN = 0), the internal oscillator frequency may shift, device current consumption can increase, and a Brown-out Reset may occur.

Work around

Set the FVREN bit of FVRCON to enable the module prior to adjusting the amplifier output selections with the CDAFVR and ADFVR bits. If switching from the 4x output setting to the 1x output setting, select the 2x output setting as an intermediary step. Always set the amplifier output selections to off ('00') before disabling the FVR module.

Affected Silicon Revisions

A4	A5						
X	X						

6. Module: ECCP

6.1 Compare Mode

The ECCP Compare Toggle mode (CCP1M<3:0> bits = 0010) works properly as long as the Timer1 Prescaler value is configured to 1:1. When the Timer1 prescaler value is configured to any other value, the ECCP Compare output yields unexpected results.

Work around

Only use the Compare Toggle mode when the Timer1 Prescaler value is set to 1:1.

Affected Silicon Revisions

A4	A5						
X	X						

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001441**F**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

None.

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APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (02/2012)

Initial release of this document.

Rev B Document (02/2013)

Added MPLAB X IDE; Added Silicon Revision A5; Added Module 2, Resets.

Data Sheet Clarifications: Removed Module 1 (Oscillator); Added new Module 1, Electrical Specifications.

Rev C Document (11/2014)

Added Module 3, MSSP; Other minor corrections.

Data Sheet Clarifications: Removed Module 1, Electrical Specifications.

Rev D Document (07/2015)

Added Modules 3.2 to 3.4 (MSSP); Removed Module 1.1 (Oscillator: HFINTOSC Ready/Stable Bit).

Rev E Document (05/2016)

Removed Module 2 (Resets); Added Modules 1.3, 3, 4, 5 and 6. Other minor corrections.

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