Erratum A-007207: TBI LINK STATUS SGMII STAYS UP

PB #16225

Affected Devices: 8156 8313 8315 8378 8533 8544 8535 8536 8569 8572 P1010 P1020 P1022 P1023 P2020

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TBI link status may stay “up” after SGMII electrical idle detected

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Description:

The TBI Status Register (SR) contains a link status bit (TBI SR [Link Status]) that represents the current state of the SGMII link. If Auto-Negotiation (AN) is disabled, the TBI link status bit should become a b’1 indicating the link is up after recognizing IDLE sequences, and stay at b’1 as long as valid data is received & the TBI is not reset. TBI link status bit should become a b’0 indicating the link is down after several invalid characters are received or the TBI is reset. If AN is enabled, the TBI link status bit does not become set to b’1 until auto-negotiation is complete (TBI CR [AN DONE]=1), but the same conditions as AN disabled then apply for the TBI link status bit to get cleared to b’0.

An electrical idle (common mode) condition on the SGMII link results in the reception of invalid data, and should cause the TBI link status bit to get cleared. If the transition from active to common mode takes enough time that the Rx is able to recognize at least 4 more K28.5 characters (for IDLE sequences, 70-80 UI), the portion of the design intended to detect the link down condition may shut off before the link down condition is actually reflected in the TBI.

This premature shutdown may cause the TBI link status to remain set to a b’1 indicating the link is up. This 'stuck at 1' condition would persist until valid K28.5 characters are received again.

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TBI link status may stay “up” after SGMII electrical idle detected (cont. 2 of 4)

Impact:

If the system never enters SGMII electrical idle, or if the transition from active to common mode takes less than 40 UI (~32 ns), then there is no impact and the false link up scenario does not occur.

If the system can generate an SGMII electrical idle condition as described above, then the TBI status may stay stuck at 1 while the link is down and does not transition to 0 until valid K28.5 characters are received again.

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TBI link status may stay “up” after SGMII electrical idle detected (cont. 3 of 4)

Workaround:
For affected systems, there is no access to electrical idle detection circuitry in SGMII mode and there is no bit replacement for TBI SR[Link Status] to monitor.

When the TBI link status is set, the SW can periodically poll the state of the Ethernet Controller by reading RBYT. If the controller is expected to receive data packets, RBYT should increment. If RBYT has not incremented over a period of time it could indicate the link is down. However, there are various reason why RBYT may not increment (controller configuration errors, SerDes PLL issues, or MIB Counter RCDE incremented). Examination of system conditions may be necessary to determine why RBYT has not incremented.

The link is down if TBI SR[Link Status]=0.

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Disposition:

No plans to fix.


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